Accurate *ac* Transistor Characterization to 110 GHz Using a New Four-port Self-Calibrated Extraction Technique

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Abstract—A new self-calibrated extraction technique for transistor characterization to 110 GHz is presented. This technique offers an on-wafer, four-port extraction approach which greatly improves the measurement accuracy at high frequencies (e.g., f > 30 GHz). In contrast to conventional parasitics-deembedding methodologies (i.e., "open-short"), the present technique requires no additional calibration (e.g., SOLT, LRRM, or TRL) before measurements. The proposed method is first simulated, and then applied to 110 GHz S-parameter measurements of state-of-the-art SiGe HBTs to demonstrate its utility. The results both theoretically and experimentally show that the proposed method represents a robust, self-calibrated approach for obtaining better accuracy in mm-wave transistor characterization.

I. Introduction

In high-frequency *ac* transistor characterization, one of the key concerns is obtaining accurate measured data. In the RF to mm-wave frequency range (1-100 GHz), the measurement of the device-under-test (DUT) is susceptible to both system-induced errors and on-wafer parasitic errors. The system-induced errors include cross-talk, mismatch, and power losses on the signal paths [1]-[3], while the on-wafer parasitics include pad capacitance, wire impedance, and other metal-to-metal interconnects (e.g., vias) [4]. To extract the intrinsic *ac* parameters from raw measured data which inherently contains these errors and parasitics, a commonly-used method is first to measure various calibration standards (i.e., SOLT, LRRM, or TRL) to calibrate the system-induced errors [5]-[7], and then measure on-wafer test structures such as an "open" and "short" to deembed the parasitics [4][8]. This technique is stable and offers acceptable accuracy at lower frequencies (f < 30 GHz). As the frequency increases, however, the parasitics-deembedding method (e.g., "open-short") begins to lose accuracy because it assumes a lumped-element equivalent model which can not capture the distributive nature of the parasitics. Moreover, "poor calibration" associated with less-than-pristine calibration hardware (e.g., ISS substrates) can also degrade the overall accuracy of the measured data.

In this paper, a extraction technique using a new four-port methodology [9] is presented. The four-port model considers distributive effects and can be used to greatly improve the accuracy of measured data at mm-wave frequencies. Furthermore, the proposed model can also capture the system-induced errors, meaning that no calibration procedure is required in the extraction. Therefore, the present method decreases the length of the measurement cycle and eliminates any potential error which may be induced during the calibration.

II. Theory

The system-induced errors in S-parameter VNA (vector network analyzer) measurements can be modeled as 12 different contributing terms [2], 6 in each direction (forward or reverse): the cross-talk of the power coupler (directivity); the cross-talk inside the S-parameter test set (crosstalk overlying the DUT); multiple reflections due to non-Z_0 input and output impedance of the cables and connectors (source and load mismatch); and the frequency dependence of the signal path R1→A and R1→B (reflection tracking A/R1 and transmission tracking B/R1). Fig. 1 shows the 6 error contribution terms in the forward direction [2].

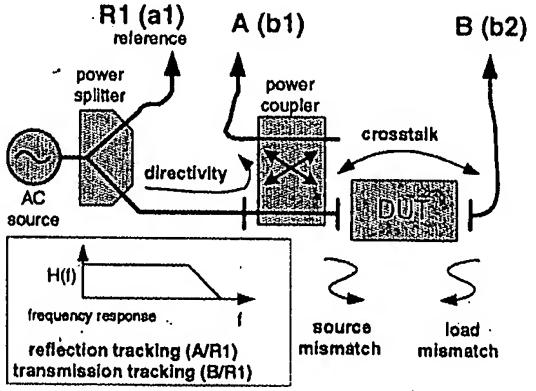

Fig. 1. The 6 error contributions for S-parameter measurements using a VNA [2].

In addition to the system-induced errors, the on-wafer parasitics, including the pad-substrate capacitance and wire impedance, are significant at high frequencies, as shown in Fig. 2. These errors and parasitics are approximately linear in *ac* measurements. Therefore, in two-port system measurements, one can summarize them into a linear four-port black-box model regardless of their different origins and mechanisms [3][9].

Fig. 3 shows the four-port equivalent model of the errors and parasitics. The port 1 and port 2 are non-physical equivalent

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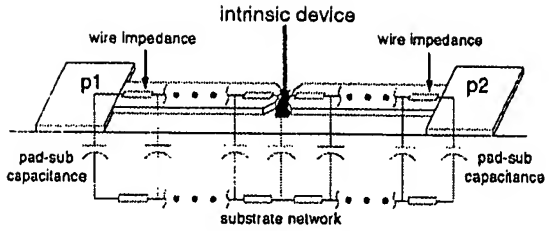

Fig. 2. The on-wafer parasitics of a 2-port system.

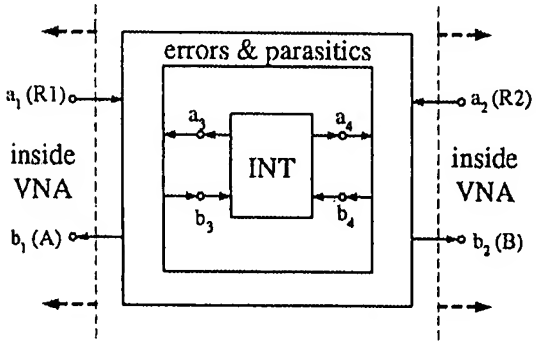

Fig. 3. Illustration of a four-port equivalent model of the errors and parasitics. The two extrinsic equivalent ports are denoted port 1 and 2, and the two ports of intrinsic device (INT) are denoted port 3 and 4.

ports. Reflectometers R1 and A measure the incoming wave and outgoing wave vectors of port 1, and reflectometers R2 and B measure the incoming wave and outgoing wave vectors of port 2, respectively. The reference planes of port 3 and port 4 are at the input and output of the intrinsic device. Thus, the errors and parasitics can be modeled as a 4 × 4 S-parameter matrix:

$$\begin{pmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{pmatrix} = \begin{bmatrix} s_{11} & s_{12} & s_{13} & s_{14} \\ s_{21} & s_{22} & s_{23} & s_{24} \\ s_{31} & s_{32} & s_{33} & s_{34} \\ s_{41} & s_{42} & s_{43} & s_{44} \end{bmatrix} \begin{pmatrix} a_1 \\ a_2 \\ a_3 \\ a_4 \end{pmatrix}. \quad (1)$$

From this, the relationship between the S-parameter observed in the VNA (S^{RAW}) and the S-parameter of intrinsic device (S^{INT}) can be derived as

$$S^{INT} = \left[S_{ir}\left(S^{RAW} - S_{rr}\right)^{-1} S_{rl} + S_{ll}\right]^{-1}, \quad (2)$$

where

$$S_{rr} = \begin{bmatrix} s_{11} & s_{12} \\ s_{21} & s_{22} \end{bmatrix}, \quad S_{rl} = \begin{bmatrix} s_{13} & s_{14} \\ s_{23} & s_{24} \end{bmatrix},$$

$$S_{ir} = \begin{bmatrix} s_{31} & s_{32} \\ s_{41} & s_{42} \end{bmatrix}, \quad S_{ll} = \begin{bmatrix} s_{33} & s_{34} \\ s_{43} & s_{44} \end{bmatrix}.$$

Previous work [9] presented a method to obtain the 4 × 4 matrix using various on-wafer test structures, and thus the required extractions are straightforward.

III. Extraction Procedure

Five different on-wafer test structures are used to extract the 4×4 matrix. Fig. 4 illustrates the layouts of the DUT and the test structures. To minimize the substrate coupling, TaN resistors are used in the left and right test structures. Since the measured device size is typically within tens of micro-meters, the distributive effect of the intrinsic resistor and intrinsic metal lines of the "short" and "through" structures can be neglected at mm-wave frequencies.

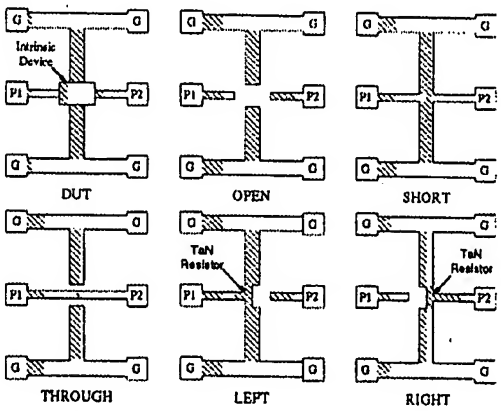

Fig. 4. The layouts of the DUT and the required test structures.

The resistance in the "left" and "right" structures can be extracted using *dc* or low frequency *ac* measurements. The 4 × 4 matrix can then be extracted using the measured S-parameters on these test structures: $[S^{OPEN}]$, $[S^{SHORT}]$, $[S^{THRU}]$, $[S^{LEFT}]$, and $[S^{RIGHT}]$. The detailed derivations and final expressions are given in reference [9].

IV. High-Frequency Measurements

The present method was first theoretically proven to work using simulations [9]. We then applied the technique to actual 2–110 GHz S-parameter measurements of state-of-the-art SiGe HBTs. The measured device is a 0.2 × 2.5 μm^2 high-performance *npn* SiGe HBT with a peak f_T of 110 GHz at J_C = 7.0 mA/μm^2. Fig. 5 shows the extracted f_T and f_{max} as a function of current density using the present method.

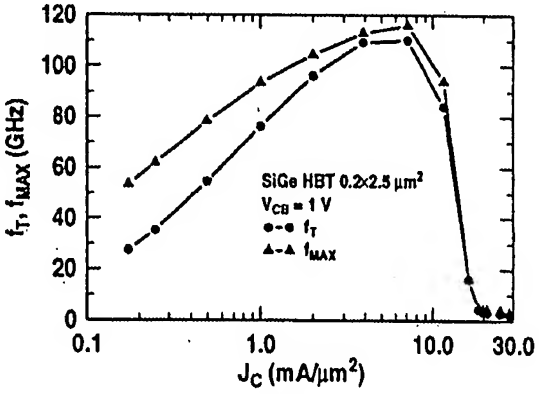

Fig. 5. The extracted f_T and f_{max} as a function of current density using the present method.

For comparison, we first used a conventional ISS calibration together with an "open-short" deembedding method (denoted "open-short"), and then the present method (denoted "four-port") on the measured S-parameters without any calibration. In

the "open-short" measurement, the Load-Reflective-Reflective-Match (LRRM) method [7] was chosen to maintain a good calibration in a wide frequency range (i.e., 2–110 GHz).

Fig. 6 shows the calibrated DUT (but not deembedded) and extracted S-parameters using the conventional "open-short" and the new "four-port" method. For a better comparison, we have plotted $S_{21}/6$ and $S_{11} - 0.75$ instead of S_{21} and S_{11}. Observe that there are large deviations between the un-deembedded and deembedded data, indicating that the on-wafer parasitics are significant in this SiGe technology. Note, however, that the deembedded S-parameters using the two methods are in close agreement, except in the high frequency range, implying the validity of both two methods at low frequencies.

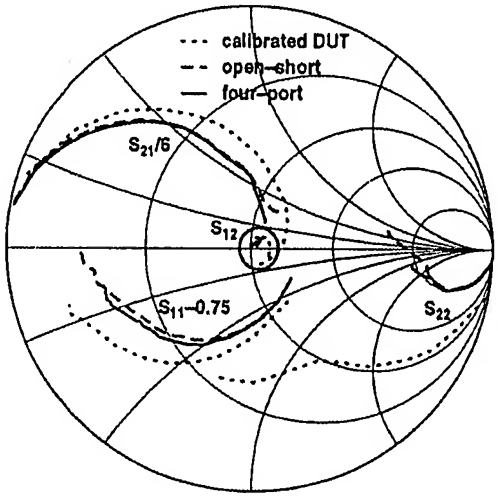

Fig. 6. The calibrated DUT and deembedded S-parameters (using "open-short" and "four-port" methods) as a function of frequency. The device was biased at $V_{be} = 0.9$ V, $V_{cb} = 1$ V.

To more closely examine the differences between the two methods, we plot the deembedded Y_{21} as a function of frequency, as shown in Fig. 7. The deviation of the results is negligible at frequencies lower than about 30 GHz. As the frequency gets higher than about 30 GHz, however, the "open-short" method overestimates the magnitude and underestimates the phase of Y_{21}. This is caused by the distributive nature of the wire lines between the pads and the intrinsic device. As expected, the error increases as the frequency increases.

These errors can severely distort the measured characteristics of the device (e.g., the gain) at high frequencies and are thus important for technology figure-of-merit characterization and accurate compact modeling. Fig. 8 shows the current gain H_{21} as a function of frequency at different bias points. Although the current gain extracted using the two methods nearly overlap at lower frequencies (the "open-short" deembedded gain is slightly less than the "four-port" gain), at frequencies above 70 GHz, the current gain extracted with the "open-short" method ceases to decrease, which is clearly not the physical (real) behavior of the intrinsic device. Observe, however, that the current gain with the present "four-port" method continues decreasing with a constant slope that approximately equals 20 dB per decade, indicating the accuracy of this technique.

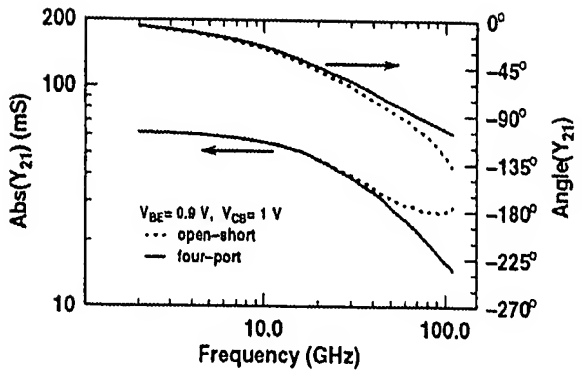

Fig. 7. The deembedded Y_{21} as a function of frequency. The device was biased at $V_{be} = 0.9$ V, $V_{cb} = 1$ V.

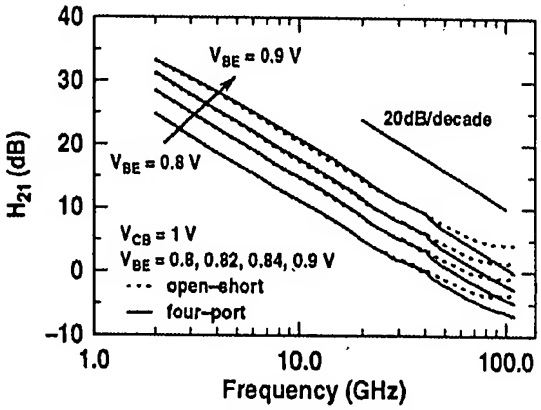

Fig. 8. The extracted current gain H_{21} as a function of frequency at different bias points.

There are deviations between the "open-short" and "four-port" results for the extracted unilateral gain G_U, the maximum available gain G_{MAG}, and the maximum stable gain G_{MSG} at high frequencies as well. However, the deviations in these gains are smaller than for the current gain. This is due to the cancellation between the errors of each Y-parameter (i.e., Y_{11} and Y_{22}). Also note that the slope of unilateral gain decreases as a function of the frequency for both methods at a rate close to 20 dB per decade (18 – 19 dB/decade), which provides a valid f_{MAX} extraction.

The transistor base resistance was used as an additional vehicle of the comparison of the conventional and new S-parameter measurement technique. In this work, the base resistance was extracted using an improved circle impedance method [10]. The $1/(Y_{11} + Y_{12})$ instead of $1/Y_{11}$ was used to exclude the effect of extrinsic collector-base capacitance. Fig. 10 shows the extracted base resistance as a function of current density J_C. There are significant deviations of R_B (5 – 10 Ω) between the two methods at low current densities, but negligible deviations at high current densities. This is because at low current densities, the base-emitter diffusion capacitance is small and thus Y_{11} is small; hence, the on-wafer parasitics are significant. At high current densities, however, the diffusion capacitance increases dramatically and thus the effect of parasitics is much smaller.

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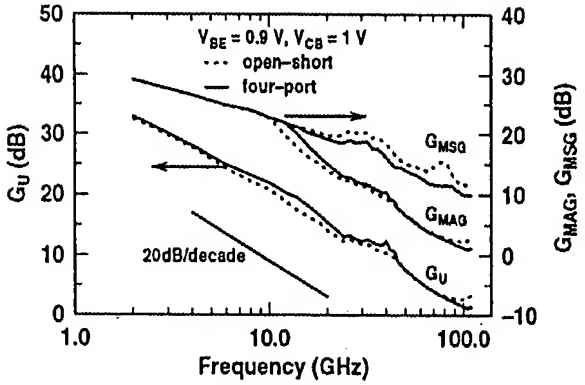

Fig. 9. The extracted unilateral gain G_U, maximum available gain G_{MAG}, and maximum stable gain G_{MSG} as a function of frequency. The device was biased at V_{be} = 0.9 V, V_{cb} = 1 V.

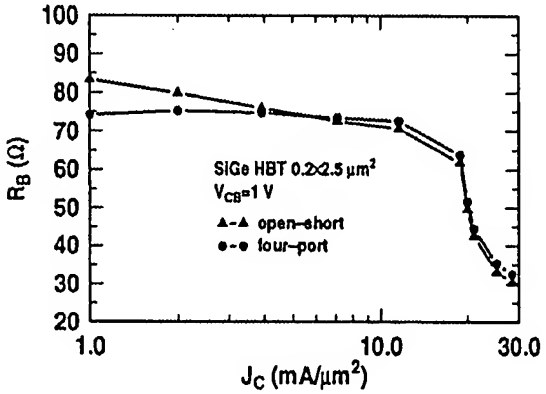

Fig. 10. The extracted base resistance as a function of current density J_C.

V. Self-Calibration Check

To check the capability of self-calibration, we applied the present "four-port" technique to both uncalibrated and calibrated (using LRRM) S-parameters. In theory, the results extracted using above measurement data should overlap if the "four-port" method can calibrate the system errors as accurately as LRRM. Fig. 11 shows the extracted S-parameters using the uncalibrated and calibrated data. Observed that the two S-parameter data overlap nicely, which implies that the present technique represents a robust self-calibrated approach.

VI. Summary

We have presented a simple, robust, self-calibrated extraction technique for transistor measurements to 100 GHz. This technique uses a four-port methodology, and greatly improves the accuracy of measurements at high frequencies (e.g., $f >$ 30 GHz). It also decreases the measurement cycle time and excludes the dependency of calibration hardware. The technique was applied in 2–110 GHz S-parameter measurements of state-of-the-art SiGe HBTs and the results show excellent consistency with theory. This technique is thus (both theoretically and experimentally) proven to be a sound method in mm-wave *ac* transistor characterization.

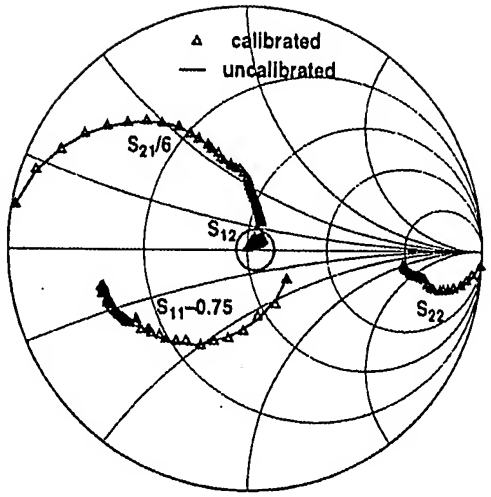

Fig. 11. The extracted S-parameters using uncalibrated and calibrated data. The device was biased at V_{be} = 0.9 V, V_{cb} = 1 V.

VII. Acknowledgment

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